FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT [redacted] IMERCE PATENT AND TRADEMARK OFFICE	ATTORN[redacted] DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371	217171US2XPCT
	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR) 09/926834

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR00/01795	27 June 2000	6 July 1999

TITLE OF INVENTION

PROCESS FOR CONTROLLING A PHOTOSENSITIVE DEVICE CAPABLE OF PRODUCING HIGH-QUALITY IMAGES

APPLICANT(S) FOR DO/EO/US

DUCOURANT Thierry et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

    PCT/IB/304/Drawings (6 sheets)
    PCT/IB/308/Form PTO-1449
    Notice of Priority

531 Rec'd PCT/PTO 28 DEC 2001

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/926834	PCT/FR00/01795	217171US2XPCT

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		CALCULATIONS PTO USE ONLY
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1040.00	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	$890.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$740.00	
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$710.00	
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =		$890.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		$0.00

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	22 - 20 =	2	x $18.00	$36.00
Independent claims	1 - 3 =	0	x $84.00	$0.00
Multiple Dependent Claims **(check if applicable)**.			☐	$0.00
TOTAL OF ABOVE CALCULATIONS			=	$926.00
☐ Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				$0.00
SUBTOTAL			=	$926.00
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	$0.00
TOTAL NATIONAL FEE			=	$926.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	$0.00
TOTAL FEES ENCLOSED			=	$926.00
			Amount to be: refunded	$
			charged	$

a. ☒ A check in the amount of **$926.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **15-0030** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Surinder Sachar
Registration No. 34,423

22850

Surinder Sachar
SIGNATURE

Marvin J. Spivak
NAME

24,913
REGISTRATION NUMBER

Dec. 28 2001
DATE

217171US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

THIERRY DUCOURANT ET AL : ATTN: APPLICATION DIVISION

SERIAL NO: NEW U.S. PCT APPLICATION :
(Based on PCT/FR00/01795)

FILED: HEREWITH :

FOR: PROCESS FOR CONTROLLING :
A PHOTOSENSITIVE DEVICE
CAPABLE OF PRODUCING
HIGH-QUALITY IMAGES

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to a first examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel Claims 1-22 without prejudice.

Please add new Claims 23-44 as follows:

23. (New) A process for controlling a photosensitive device including at least one photosensitive point with a photodiode connected to a switching element, comprising:

submitting the photosensitive point to successive imaging cycles,

producing between a first imaging cycle and a second imaging cycle, a holding phase terminating at a start of the second imaging cycle, during this holding phase, whose duration

is equal to several equal time intervals which are as short as possible, the photosensitive point is exposed to an optical flash at a start of each time interval and between successive optical flashes, the photodiode is reverse biased, the junction region between the photodiode and the switching element having substantially a same potential at an end of each time interval.

24. (New) The control process as claimed in claim 23, wherein an imaging cycle comprises an imaging phase followed by a phase of reading an amount of charge accumulated in the junction region during the imaging phase, the read phase being followed by an erasure and reinitialization phase, during which the photosensitive point is exposed to an optical erasure flux causing the photodiode to conduct in a forward direction, and the photodiode to be reverse biased at an end of the erasure and reinitialization phase.

25. (New) The control process as claimed in claim 24, wherein the imaging cycles are requested by an operator, and further comprising synchronizing the start of an imaging cycle with an end of the time interval during which the operator's request occurs.

26. (New) The control process as claimed in claim 23, wherein the frequency of the optical flashes is synchronized with that of mains.

27. (New) The control process as claimed in claim 23, further comprising applying a biasing pulse to the photosensitive point for an entire duration of the holding phase.

28. (New) The control process as claimed in claim 24, further comprising, during the erasure and reinitialization phase, applying to the photosensitive point a biasing pulse starting before the end of the exposure to the optical erasure flux and continuing thereafter.

29. (New) The control process as claimed in claim 28, wherein the biasing pulse of the erasure and reinitialization phase is continued during the holding phase.

30. (New) The control process as claimed in claim 24, further comprising, during the erasure and reinitialization phase, before the exposure of the photosensitive point to the optical erasure flux, exposing the photosensitive point at least once to an optical pre-erasure flux causing the photodiode to conduct in the forward direction.

31. (New) The control process as claimed in claim 30, wherein the exposure of the photosensitive point to the optical pre-erasure flux is followed by the reverse biasing of the photodiode, the reverse biasing of the photodiode occurring before exposure to the optical erasure flux.

32. (New) The control process as claimed in claim 31, further comprising applying to the photosensitive point a biasing pulse starting after the end of the exposure to the optical pre-erasure flux and terminating before the start of the exposure to the optical erasure flux.

33. (New) The control process as claimed in claim 23, further comprising starting the holding phase as quickly as possible after the end of the first imaging cycle.

34. (New) The control process as claimed in claim 24, further comprising, during the read phase, applying to the photosensitive point a read pulse having a same sign as and an amplitude greater than or equal to the biasing pulse.

35. (New) The control process as claimed in claim 23, wherein the switching element is a diode.

36. (New) The control process as claimed in claim 23, wherein the switching element is a transistor.

37. (New) The control process as claimed in claim 23, wherein the photosensitive point is produced on a first face of a substrate transparent to light, and further comprising applying the optical flashes to the photosensitive point through the transparent substrate.

38. (New) The control process as claimed in claim 24, further comprising using a same source to deliver the optical flashes and the optical erasure flux.

39. (New) A photosensitive device implementing the control process as claimed in claim 26, comprising at least one photosensitive point with a photodiode connected to a switching element, means for exposing the photosensitive point to a series of periodic optical flashes, and means to reverse bias the photodiode at an end of an optical flash so that it is in a receptive state from a start of a second imaging cycle.

40. (New) The device as claimed in claim 39, wherein the means to reverse bias the photodiode is configured to apply to the photosensitive point a biasing pulse during the exposure to the series of optical flashes.

41. (New) The device as claimed in claim 39, wherein the switching element is a diode.

42. (New) The device as claimed in claim 39, wherein the switching element is a transistor.

43. (New) The device as claimed in claim 39, wherein the photosensitive point is produced on a first face of a substrate transparent to light and further comprising a source for delivering the optical flashes, placed on the second face of the substrate.

44. (New) The photosensitive device as claimed in claim 39, further comprising a scintillator converting X-ray radiation incident on taking the image into optical radiation, the photodiode being sensitive to the optical radiation.

IN THE ABSTRACT OF THE DISCLOSURE

Please amend the Abstract on page 24 as follows:

ABSTRACT

A process for controlling a photosensitive device including at least one photosensitive point with a photodiode connected to a switching element. The process submits the photosensitive point to successive imaging cycles. Between a first imaging cycle and a second imaging cycle, the process produces a holding phase terminating at the start of the second imaging cycle. During this holding phase, whose duration is equal to several equal time intervals that are as short as possible, the photosensitive point is exposed to an optical flash at the start of each time interval. Between successive optical flashes, the photodiode is reverse biased. The junction region between the photodiode and the switching element has substantially the same potential at the end of each time interval.

REMARKS

Favorable consideration of this application, as presently amended, is respectfully requested.

The present preliminary amendment is submitted to place the above-identified application in more proper format under United States practice.

By the present preliminary amendment original Claims 1-22 are cancelled and new Claims 23-44 are presented for examination. New Claims 23-44 are believed to be self-evident from the original disclosure, including original Claims 1-22, and thus are not deemed to raise any issues of new matter.

New Claims 23-24 have been written to correct minor informalities, without narrowing the scope of the claims. Moreover, new Claims 23-24 no longer recite any

reference numerals and no longer recite the close-ended term "consisting", but instead recite the broader open-ended term "comprising". In such ways, the differences between new Claims 23-44 and original Claims 1-22 are deemed to only broaden the scope of new Claims 23-44.

The Abstract has also been amended by the present response to be in more proper format under United States practice.

The present application is believed to be in condition for a full and thorough examination on the merits. An early and favorable consideration of the present application is hereby respectfully requested.

Respectfully submitted,

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217171US

Marked-Up Copy
Serial No:
Amendment Filed on:
12-28-2001

IN THE CLAIMS

Please cancel Claims 1-22 without prejudice.

Please add new Claims 23-44 as follows:

IN THE ABSTRACT OF THE DISCLOSURE

Please amend the Abstract on page 24 as follows:

--ABSTRACT

[PROCESS FOR CONTROLLING A PHOTOSENSITIVE DEVICE CAPABLE OF PRODUCING HIGH-QUALITY IMAGES]

A process for controlling a photosensitive device [comprising] including at least one photosensitive point [(P1 to P9)] with a photodiode [(Dp)] connected to a switching element [(Dc, T)]. [It consists in submitting] The process submits the photosensitive point to successive imaging cycles. Between a first imaging cycle and a second imaging cycle, [it consists in producing] the process produces a holding phase [(PHM)] terminating at the start of the second imaging cycle. During this holding phase [(PHM)], whose duration is equal to several equal time intervals [(dt) which] that are as short as possible, the photosensitive point is exposed to an optical flash [(FO)] at the start of each time interval. Between [the] successive optical flashes, the photodiode is reverse biased. The junction region between the

photodiode and the switching element has substantially the same potential [(VA)] at the end of each time interval [(dt)].

[Figures: 3a to 3e]--

PROCESS FOR CONTROLLING A PHOTOSENSITIVE DEVICE CAPABLE OF PRODUCING HIGH-QUALITY IMAGES

The present invention relates to a process for controlling a photosensitive device consisting of at least one photosensitive point produced by techniques for depositing semiconductor materials such as amorphous silicon. The aim of the invention is to enable images to be taken at random times, the imaging produced by the photosensitive device having as good a quality as possible especially in terms of remanence and stability.

More particularly but not exclusively, the invention relates to the control of such devices used in the detection of radiological images.

In order to use these photosensitive devices in the detection of radiological images, a scintillator is inserted between the photosensitive device and the X-ray radiation in order to convert the X-ray radiation into optical radiation in the wavelength band to which the photosensitive point is sensitive. The scintillator material is generally cesium iodide, which is known for its low intrinsic remanence.

A photosensitive point generally comprises a photodiode combined with a switching element having a switching function. The photodiode at least is made from an amorphous semiconducting material. The photosensitive point is mounted between a row conductor and a column conductor. According to requirements, the photosensitive device then comprises a plurality of photosensitive points arranged in a matrix or in a linear array.

The amorphous semiconducting material produces the remanence. This is linked to its amorphous structure which comprises a large number of traps, many more than

in crystalline materials. These traps are structural defects which extend throughout the bandgap. They retain charges generated on taking an image. The material stores an image corresponding to a given radiation and restores charges relating to this image on reading the following image or even several following images. The quality of the images thereby suffers.

Another defect affects the quality of the images. The semiconductor components used in such photosensitive devices are not all identical and the photosensitive device has inherent inhomogeneities which result in impaired regions and which vary over time.

To try to obtain a useful image of optimal quality, the useful image is corrected from an image called an "offset image", also known as a black image, generally taken and stored at the start of an operating cycle. This offset image is the image obtained when the photosensitive device is exposed to a signal of zero intensity and corresponds to a sort of background image. The offset image varies depending on the electrical state of the components of the photosensitive points and of the dispersion of their electrical characteristics.

The useful image is that read when the photosensitive device has been exposed to a useful signal which corresponds to an exposure to X-ray radiation. It encompasses the offset image.

The correction consists in carrying out a subtraction between the useful image and the offset image. This correction is only reliable if the offset image has not varied between the moment where it was taken and the moment where the useful image is taken. It is necessary for the photosensitive points to be in the same electrical state just before taking the offset image

and before taking the useful image. In the absence of control, the semiconductor components are continuously searching for an equilibrium state which may be reached in a few hours since the time taken to fill the traps and that taken to empty them of stored charges spreads out over time ranges of between a few microseconds and a few minutes or even a few hours. After this period of time their state may still vary depending on the temperature or on infinitesimal variations of residual irradiation.

Since the offset image is generally taken at the start of the operating cycle of the photosensitive device and since the useful image, actuated at the discretion of the radiologist, is taken randomly as needed, there is no reason for all the semiconductor components to be in the same state at these two times which are separated by a variable time interval.

Figures 1a, 1b symbolize of the the fill state of the traps of the components of a photosensitive point of a photosensitive device to which the invention may be applied, over time. The arrows represent imaging cycles. The term "imaging cycle" refers to the sequence consisting of an imaging phase followed by a read phase then by an erasure and reinitialization phase, as explained in Patent Application FR-A-2 760 585. During the imaging phase, the photosensitive points are exposed to a signal to be picked up, whether this signal is at maximum illumination or darkness, during the read phase a read pulse is applied to the addressed row conductors in order to read the amount of charge accumulated on taking the image. During the erasure and reinitialization phase, the photosensitive points are erased, generally optically, and returned to a state in which they are receptive to new imaging.

Between two successive imaging cycles, the photosensitive points are left at rest, but their

electrical state changes. It is assumed that the first imaging cycle represented provides the offset image and the others, useful images to be corrected with the offset image.

It can be clearly seen that if the imaging cycles occur randomly, as in figure 1a, the electrical states of the photosensitive point being different at the start of the cycle, the useful images corrected with the offset image cannot be reliable.

On the other hand, in figure 1b, the imaging cycles occur regularly, for example every five seconds, and at the start of each cycle the electrical state of the photosensitive point is substantially the same.

The offset image has not fluctuated and the correction of a useful image taken during a cycle with the offset image taken during another preceding cycle, is reliable. The major drawback of this operating mode is that it brings many constraints, since the various cycles must follow one another periodically in order to obtain the expected result.

This use is very restrictive and is not compatible with the expectations of radiologists who wish to be able to request images as needed. The present invention proposes to avoid this major drawback while guaranteeing an image of optimum quality.

According to the invention, a process for controlling a photosensitive device comprising at least one photosensitive point with a photodiode connected to a switching element, consists in submitting the photosensitive point to successive imaging cycles and between a first imaging cycle and a second imaging cycle, in producing a holding phase terminating at the start of the second imaging cycle. During this holding phase, whose duration is equal to several equal time

intervals which are as short as possible, the photosensitive point is exposed to an optical flash at the start of each time interval and between the successive optical flashes, the photodiode is reverse biased, the junction region between the photodiode and the switching element having substantially the same potential at the end of each time interval.

An imaging cycle comprises an imaging phase followed by a phase of reading the amount of charge accumulated in the junction region during the imaging phase, the read phase being followed by an erasure and reinitialization phase, during which the photosensitive point is exposed to an optical erasure stream causing the photodiode to conduct in the forward direction, and the photodiode to be reverse biased at the end of the erasure and reinitialization phase.

During the operation of such devices, it is an operator who requests an image and some delay may appear between the request and the start of the corresponding imaging cycle, since the start of the imaging cycle is designed to be synchronized with the end of the time interval during which the operator's request occurs.

In order to overcome possible problems of electrical disturbances it is preferable for the frequency of the optical flashes to be that of the mains used, for example 50 Hz or 60 Hz.

It is preferable to leave the photosensitive point in the biased state for the entire duration of the holding phase, for the purpose of simplifying the control circuits.

With the same aim, during the erasure and reinitialization phase, it is preferable to apply to the photosensitive point a biasing pulse starting

before the end of the exposure to the optical erasure flux and continuing thereafter.

During the erasure and reinitialization phase, before the exposure of the photosensitive point to the optical erasure flux, it is possible to expose it at least once to an optical pre-erasure flux causing the photodiode to conduct in the forward direction so as to improve the erasure, when very low remanence levels are required.

The exposure of the photosensitive point to the optical pre-erasure flux is followed by the reverse biasing of the photodiode, this reverse biasing of the photodiode occurring before exposure to the optical erasure flux.

The holding phase starts as quickly as possible after the end of the first imaging cycle so as to keep the photosensitive point substantially in the same state at the start of the holding phase as at the end of the first imaging cycle.

During the read phase, a read pulse having the same sign as and an amplitude greater than or equal to the biasing pulse is applied to the photosensitive point.

The present invention also relates to a photosensitive device implementing the control process. It comprises at least one photosensitive point with a photodiode connected to a switching element, means for exposing the photosensitive point to a series of periodic optical flashes and means to reverse bias the photodiode at the end of an optical flash so that it is in a receptive state from the start of the second imaging cycle.

Other characteristics and advantages of the invention will appear on reading the following detailed

description, made by way of nonlimiting examples with reference to the appended drawings in which:

- figures 1a, 1b, already described, show the state of the traps of the components of a photosensitive point when it is used according to known procedures;
- figure 2 shows a photosensitive device to which the process of the invention may be applied;
- figures 3a to 3e show timing diagrams illustrating the operation of the photosensitive device of figure 2 under the control of the process of the invention;
- figures 4a to 4d show timing diagrams illustrating the operation of the device of figure 2 under the control of a variant of the process of the invention;
- figure 5 shows a variant of a photosensitive device to which the process of the invention may be applied;
- figures 6a to 6d show timing diagrams illustrating the operation of the photosensitive device of figure 5 under the control of the process of the invention.

Figure 2 shows schematically an example of a photosensitive device 2 to which the process of the invention may be applied. It comprises photosensitive points arranged in a matrix and referenced P1 to P9. Each photosensitive point consists of a photodiode Dp and a switching diode Dc assembled in series in a back-to-back configuration. The matrix comprises row conductors Y1 to Y3 intersecting with column conductors X1 to X3, with a photosensitive point connected between a row conductor and a column conductor at each intersection. The photosensitive points P1 to P9 are thus placed along rows L1 to L3 and columns CL1 to CL3.

In the example of figure 2, only three rows and three columns are shown and they define nine photosensitive points, but such a matrix may have a much larger capacity, possibly going up to several million points.

For example, it is common to produce such matrices having photosensitive points placed along 2000 rows and 2000 columns (over an area of about 40 cm x 40 cm) or even arranged over a single row and several columns in order to form a linear detection array, or even arranged over a single row and a single column in order to form a single photosensitive point.

The photosensitive device comprises a row control circuit 3, the outputs SY1, SY2, SY3 of which are connected to the row conductors Y1, Y2, Y3, respectively. The row control circuit 3 has various elements (not shown), such as for example, a clock circuit, switching circuits, shift register, which enable it in particular to address row conductors Y1 to Y3 sequentially. At each photosensitive point P1 to P9, the two diodes Dp, Dc are connected to each other either by their cathode, or by their anode, as in the example shown. The cathode of the photodiode Dp is connected to a column conductor X1 to X3, and the cathode of the switching diode Dc is connected to a row conductor Y1 to Y3.

The column conductors X1 to X3 are connected to a read circuit CL, in the example comprising an integrator circuit 5 and a multiplexer circuit 6. Each column conductor is connected to a negative input "-" of an amplifier G1 to G3 mounted as an integrator. An integrating capacitor C1 to C3 is mounted between the negative input "-" and an output S1 to S3 of each amplifier. The second input "+" of each amplifier G1 to G3 is connected to a potential which, in the example, is the reference potential VR, a potential which is subsequently applied to all the column conductors X1 to X3. Each amplifier comprises a switching element I1 to I3, called a "reset element" (for example consisting of a transistor of the MOS type), mounted in parallel with each integrating capacitor C1 to C3.

The outputs S1 to S3 of the amplifiers are connected to the inputs E1 to E3 of the multiplexer 6. This conventional arrangement makes it possible to deliver "in series" and row after row (L1 to L3), at the output SM of the multiplexer 6, signals which correspond to the charges accumulated at the points "A" of all the photosensitive points P1 to P9.

It should be noted that it is also known for a transistor to be used to fulfil the switching function which, in the example of figure 2, is held by the switching diode Dc; compared to the diode, the latter is more complex to connect, but it offers advantages in the quality of its "on" state, advantages which will be mentioned in the rest of the description.

The development of the control process according to the invention, with two imaging cycles separated by a holding phase, will now be described, taking the photosensitive device of figure 2 as an example, each photosensitive point of which comprises a switching diode Dc to fulfil the switching function. Figures 3 are time diagrams of the various events relating to the control process according to the invention. Figure 3a illustrates the imaging phases PHI, figure 3b shows the signals applied to a row conductor, Y1 for example, especially for the purpose of reading, figure 3c the erasure signals of a photosensitive point P1 for example, figure 3d the variations in the voltage VA at the point "A" which is at the junction between the photodiode and the switching element of the point P1 and figure 3e makes it possible to locate the times during which the reset switches I1 to I3 go from the closed state (0) to the open state (1) so as to enable the charges read to be integrated in the open state by the amplifiers G1 to G3.

In the nonlimiting example described we start at time t0 by the start of a first imaging cycle firstly

comprising an imaging phase PHI in which the photosensitive point P1 will be exposed to a signal to be picked up, this imaging phase PHI is followed by a read phase PHL. The two diodes Dp, Dc of the photosensitive point P1 in question are reverse biased, and in this state each one constitutes a capacitor. It should be noted that generally, the two diodes Dp, Dc are designed so that the capacitor presented by the photodiode Dp is the strongest (for example, by about 50 times). The illumination is between a maximum illumination and zero illumination to the extent that the photosensitive point may remain in darkness. This is what happens especially on taking the offset image.

The illumination creates a variation (in this case an increase) in the voltage VA at the point A, this variation is connected to the amount of charge accumulated at the point A under the effect of the illumination. The voltage VA goes from VA1 at time t0 to VA2 at time t1, which marks the end of the imaging phase PHI.

Time t2 marks the start of the read phase PHL. It makes it possible to read the amount of charge accumulated at the point A during the imaging phase PHI which has just taken place. The photosensitive points P1 to P9 are read row by row, simultaneously for all the photosensitive points P1 to P9 connected to the same row conductor Y1 to Y3. To this end, the row control circuit 3 applies a pulse IL called a "read pulse" with a given amplitude VP2 to each addressed row conductor Y1 to Y3; the row conductors which are not addressed are kept at a reference potential VR or rest potential, which is for example ground, and which may be the same potential as that which is applied to the column conductors X1 to X3. A voltage source 4, delivering the voltage VP2 to the row control circuit 3, serves to define the amplitude of the read pulses IL applied to the row conductors.

For the purpose of simplification, between time t1 and time t2, we have omitted showing the effect of the darkness currents which cause the voltage VA to increase slightly. The rising edge of the read pulse IL, which has a negative sign with respect to a reference voltage VR and the amplitude VP2, has the effect of causing the switching diode DC to conduct in the forward direction and the latter charges the capacitor which constitutes the photodiode Dp. The voltage VA decreases exponentially from the voltage VA2 to the voltage VA3 at time t3 when the read pulse IL ceases and when the voltage on the row conductor Y1 returns to the reference value VR.

The switching diode Dc is put into reverse bias and forms a capacitor. At time t3, the voltage VA increases from VA3 to VA4 by capacitive division.

All the row conductors Y1 to Y3 receive a read pulse IL one after the other during this read phase PHL which ceases at time t'1 but the time diagram of figure 3b shows only the read pulse applied to the row conductor Y1.

Next, the erasure and reinitialization phase PHER starts at time t4, which aims to erase the traces of taking the previous image and to prevent any correlation between taking the previous image and taking a future image.

This phase comprises an erasure which consists in saturating the existing traps in the semiconductor material of the photodiode Dp, followed by biasing which aims to put the photosensitive points P1 to P9 in a state such that they are receptive to taking a new image, that is to say so that they can produce and accumulate charge during the taking of the new image.

The erasure is caused by exposing the photosensitive points to an optical flux FE of sufficient intensity and duration for the charges that it generates at the point "A" to cause the photodiode Dp to conduct in the forward direction.

From time t4, the voltage VA varies (by increasing) until it reaches a value VA5 before the end of the application of the erasure flux FE which corresponds to the break voltage of the photodiode Dp. The latter conducts in its forward conduction direction. The voltage VA keeps the value VA5 until time t6 which marks the start of the application, to the row conductors, of a biasing pulse IP having an amplitude VP1, which is negative with respect to the reference voltage VR, that is to say having the same direction as the read pulse IL. A voltage source 13, delivering the voltage VP1 to the row control circuit 3, serves to define the amplitude of the biasing pulses IP applied to the row conductors.

This biasing pulse IP reinitializes the photosensitive point, that is to say returns the photodiodes Dp to the reverse biased state so that they are receptive to taking a new image. They will again be able to produce and accumulate charge. Starting from time t6, the voltage VA decreases until taking the value VA1 equal to VP1 less the break voltage of the switching diode Dc at time t7. The photosensitive points P1 to P9 are then reinitialized and they have completely lost the memory of the image taken at the start of the imaging cycle at time t0. The erasure and reinitialization phase PHER is terminated together with the imaging cycle started at time t0. If a new imaging cycle does not start immediately after time t7 and if the photosensitive point P1 is no longer stimulated, the voltage VA will decrease until electrical equilibrium is reached, which may take several minutes or even a few hours, the future taking of an image will be dependent on the

duration between time t7 and time t'0 marking start of a second imaging cycle. A phase seeking electrical equilibrium then starts between the reverse current of the photodiode Dp, a relaxation current of the traps and the forward current of the switching diode Dc. The situation is then the same as that described in figure 1a if the imaging cycles are not regular.

According to a characteristic of the process subject of the invention, a holding phase PHM starts from a time t8 which follows time t7. It finishes at a time t'0 which marks the start of a second imaging cycle. The duration of the holding phase is equal to a whole number of equal time intervals dt, of a duration as short as possible, each time interval dt starts by exposing the photosensitive points to an optical flash FO, for the rest of time interval dt, the photodiodes are reverse biased. In other words, the photosensitive points are exposed to a burst of periodic optical flashes FO with a period dt which is as short as possible.

Thus, during this holding phase PHM, the photosensitive points are kept in a substantially constant electrical state.

The effect of exposing a photosensitive point to an optical flash FO is to increase the voltage VA up to a value VA7 and to fill the traps. When it ceases and the photodiode is reverse biased, the traps empty and the voltage VA decreases down to a value VA8. It is arranged that the voltage VA keeps substantially the same value VA8 at the end of each time interval dt by adjusting the respective duration of the optical flashes FO and the time intervals dt. When a new optical flash is applied, the voltage VA increases again up to VA7 and so on. The voltage VA will continue to vary between the two limits VA7, VA8 while this holding phase PHM continues. In the example illustrated

in figures 3, the reverse bias of the photodiodes Dp is obtained by maintaining a biasing pulse IP for the whole duration of the holding phase PHM. More specifically, in order to simplify the controls, it is preferable that the biasing pulse IP of the erasure and reinitialization phase PHER is continued through the entire holding phase since, as will be explained subsequently, attempts are made to start the holding phase PHM as quickly as possible after the end of the erasure and reinitialization phase PHER.

The period dt of the optical flashes is chosen to be as short as possible, for example about 60 ms, in order to allow image requests which are as asynchronous as possible. This is because, when an operator requests an image at a time t9, for example, during a time interval dt of the holding phase PHM, the start of the second imaging cycle is delayed until time t'0 which corresponds to the end of the time interval dt during which the image request occurs. Time t'0 marks the end of the optical flashes and the end of the biasing pulse IP. In other words, the imaging cycles are synchronized to the end of a time interval dt.

In order to avoid disturbances connected with the electromagnetic field originating from the mains frequency, it is possible that the time intervals dt are made synchronous with the mains. Each time interval dt then has the value, for example, of 20 milliseconds if the mains frequency is 50 Hz or 16.66 milliseconds if it has the value of 60 Hz, as in the United States.

In order to further improve the efficiency of the erasure and reinitialization phase PHER with respect to the example described in figures 3, if only very small remanence levels are tolerated, it is possible to provide, before exposure of the photosensitive points to the optical erasure flux FE, at least one exposure to an optical pre-erasure flux FEP without the

photodiodes being bias controlled. The row conductors Y1 to Y3 are at the potential VR. The optical pre-erasure flux has an intensity and a duration such that the photodiode Dp passes into forward mode. At the end of the pre-erasure FEP, the photodiodes are put into reverse bias by applying a biasing pulse IP1 on the row conductors Y1 to Y3, this pulse IP1 ceasing before exposing the photosensitive points to a new illumination, that is to say either a new pre-illumination FEP or the illumination FE. The time diagrams of figures 4a to 4d show this variant of the process according to the invention.

The imaging and read phases take place between t0 or t'0 and t3 and are similar to those of figures 3 while the erasure and the reinitialization phase PHER has been extended. The holding phase PHM is also similar to that which was described previously.

In the example of figures 4, the erasure and reinitialization phase PHER starts at time t4 with at least one exposure of the photosensitive points to an optical pre-erasure flux FEP and this until time t5. The photodiodes Dp switch to conduction in the forward direction and the voltage VA increases up to the moment where it reaches the break voltage of the photodiodes Dp and then remains substantially constant until t5 which marks the end of the exposure to the optical pre-erasure flux FEP. Time t6 marks the start of the application of a biasing pulse IP1 of amplitude VP1 that is intended to reset the photodiodes Dp into the reverse bias state so that the photosensitive points are in a state receptive to a subsequent image request. The voltage VA decreases to draw back, at time t7, which marks the end of the biasing pulse IP1, toward the voltage VP1 less the break voltage of the switching diode Dc. After time t7 the actual erasure can commence. This erasure starts at time t8 with exposure to an optical erasure flux FE. The development of the

process then corresponds to that which was described in figures 3 from time t4, except for the fact that the biasing pulse IP starts at time t9 when the erasure flux FE has not yet stopped. Between time t8 and time t9, the voltage VA increases until the photodiode Dp switches to conduct in the forward direction. Between time t9 and time t10 which marks the end of the exposure to the erasure flux FE, the voltage VA starts to decrease with a lower slope than if the biasing pulse IP was applied alone. The slope increases after time t10 since the erasure flux FE has stopped.

The voltage VA continues to decrease until reaching the voltage VP1 less the break voltage of the switching diode Dc, at time t11. From this time t11, which marks the end of the erasure and reinitialization phase PHER, the holding phase PHM is started as quickly as possible. This holding phase PHM starts at time t12. Between time t11 and time t12, the electrical state of the photodiodes varies and the voltage VA continues to decrease. The time interval between t11 and t12 is set to a maximum of, for example, 500 milliseconds, so that the voltage VA keeps a value close to that reached at the end of the erasure and reinitialization phase PHER. The value of 500 milliseconds is not limiting. The holding phase is identical to that which was described in figure 3 between times t8 and t'0.

The optical flux or the optical fluxes of the erasure and reinitialization phase are delivered by a source SL which is in itself conventional. It may be produced for example by a lumiplate, an array of light-emitting diodes or a photoluminescent film.

It may be placed against the substrate 7, away from the photosensitive points, if it is transparent to light. It may be made of glass or quartz for example. In figure 2, the source SL is represented by dotted lines, and supposing that the substrate 7 is in the plane of

the figure, it would be located behind. It could of course be located at the side of the photosensitive points, insofar as it is not detrimental to the exposure of the points on imaging.

The source SL can be controlled conventionally from a signal delivered by an output SS1 of the row control circuit 3.

The source which makes it possible to supply the optical flashes FO may be of the same nature as that SL which delivers the optical erasure fluxes. The same source SL may deliver the optical flashes and the erasure flux as illustrated in figure 2, but this is not essential and distinct sources may be provided.

The biasing pulses IP have an amplitude VP1 which is less than that VP2 of the read pulses IL as explained in French Patent Application FR-A-2 760 585. They may be applied to all the row conductors Y1 to Y3 by the row control circuit 3, either simultaneously or row by row.

Instead of the switching element Dc of the photosensitive points P1 to P9 being a switching diode as illustrated in figure 2, it is possible, as illustrated in figure 5, to replace it with a transistor T also produced by thin film deposition techniques (TFT).

In the diagram of figure 5, each transistor T is connected by its source S to the cathode of the photodiode Dp, that is to say to the point A, its gate G is connected to the row conductor Y1 to Y3 to which the photosensitive point belongs and its drain D is connected to the column conductor X1 to X3 to which the photosensitive point belongs. The anodes of all the photodiodes Dp are joined and connected to a specific supply 5' which delivers a negative biasing voltage

VBIAS of about -5 volts to -10 volts and which serves to constitute the reverse bias of the photodiodes Dp.

The row control circuit 3 delivers, via its outputs SY1 to SY3, voltage signals or pulses which, on going from VOFF to VON cause all the transistors T of a same row to pass simultaneously from the "off" state to the "on" state, respectively. The row control circuit 3 receives the voltage VON from a voltage source 4' and the voltage VOFF from a voltage source 13'. The voltage VOFF is about -10 volts while the voltage VON is about +15 volts.

Setting a transistor T to the "on" state causes the voltage VCOL, present on the column to which the drain D of the transistor T is connected, to be applied to the cathode of the photodiode Dp to which the transistor is connected. This voltage VCOL is generally about 0 volts.

The operation of the photosensitive point in question is similar to that which has just been described with the diodes.

However, the voltage VA at the junction between the photodiode Dp and the transistor T varies inversely to that of a photosensitive point with two diodes. The time diagram of figure 6d is shown as a mirror image of figure 3d. With regard to the figures 6a and 6c, they are similar to those of figures 3a and 3c.

As for figure 6b, which shows the signal applied to the row conductor of the photosensitive point in question, only the amplitude and the sign of the pulses applied vary compared with those of figure 3b. When it is not addressed, the row conductor in question is held at the potential VOFF and when it is addressed in read, it is brought by means of a read pulse IL to the amplitude VON.

Another difference to be stressed with respect to the example of figures 3 is that the biasing pulse IP preferably has the same amplitude as the read pulse IL; it is not useful to use drive charges as disclosed in Patent Application FR-A-2 760 585 since the electrical quality of a transistor with the switching function is better than that of a diode.

The process of the invention is applicable to the control of photosensitive devices used in detecting radiological images. These devices therefore comprise a scintillator in order to convert incident radiation, generally X-ray radiation, into light radiation in the band of wavelengths to which the photodiodes Dp are sensitive. On the device shown in figure 2, a scintillator 9 is symbolized by a square in dotted lines. It may be made from cesium iodide which is known for its low remanence. This scintillator 9 is deposited on the matrix 2 so as to be inserted between the latter and the incident X-ray radiation.

CLAIMS

1. A process for controlling a photosensitive device comprising at least one photosensitive point (P1 to P9) with a photodiode (Dp) connected to a switching element (Dc, T), consisting in submitting the photosensitive point to successive imaging cycles, characterized in that it consists, between a first imaging cycle and a second imaging cycle, in producing a holding phase (PHM) terminating at the start of the second imaging cycle, during this holding phase (PHM), whose duration is equal to several equal time intervals (dt) which are as short as possible, the photosensitive point is exposed to an optical flash (FO) at the start of each time interval and between the successive optical flashes, the photodiode is reverse biased, the junction region between the photodiode and the switching element having substantially the same potential (VA) at the end of each time interval (dt).

2. The control process as claimed in claim 1, characterized in that an imaging cycle comprises an imaging phase (PHI) followed by a phase (PHL) of reading the amount of charge accumulated in the junction region during the imaging phase, the read phase being followed by an erasure and reinitialization phase (PHER), during which the photosensitive point is exposed to an optical erasure flux (FE) causing the photodiode to conduct in the forward direction, and the photodiode to be reverse biased at the end of the erasure and reinitialization phase.

3. The control process as claimed in claim 2, in which the imaging cycles are requested by an operator, characterized in that it synchronizes the start of an imaging cycle with the end of the time interval during which the operator's request occurs.

4. The control process as claimed in one of claims 1 to 3, characterized in that the frequency of the optical flashes is synchronized with that of the mains.

5. The control process as claimed in one of claims 1 to 4, characterized in that it consists in applying a biasing pulse (IP) to the photosensitive point for the entire duration of the holding phase (PHM).

6. The control process as claimed in one of claims 2 to 5, characterized in that it consists, during the erasure and reinitialization phase (PHER), in applying to the photosensitive point a biasing pulse (IP) starting before the end of the exposure to the optical erasure flux (FE) and continuing thereafter.

7. The control process as claimed in claim 6, characterized in that the biasing pulse (IP) of the erasure and reinitialization phase (PHER) is continued during the holding phase (PHM).

8. The control process as claimed in one of claims 2 to 7, characterized in that it consists, during the erasure and reinitialization phase (PHER), before the exposure of the photosensitive point to the optical erasure flux, in exposing the photosensitive point at least once to an optical pre-erasure flux (FEP) causing the photodiode (Dp) to conduct in the forward direction.

9. The control process as claimed in claim 8, characterized in that the exposure of the photosensitive point to the optical pre-erasure flux (FEP) is followed by the reverse biasing of the photodiode, this reverse biasing of the photodiode occurring before exposure to the optical erasure flux (FE).

10. The control process as claimed in claim 9, characterized in that it consists in applying to the photosensitive point a biasing pulse (IP1) starting after the end of the exposure to the optical pre-erasure flux (FEP) and terminating before the start of the exposure to the optical erasure flux (FE).

11. The control process as claimed in one of claims 1 to 10, characterized in that it consists in starting the holding phase (PHM) as quickly as possible after the end of the first imaging cycle.

12. The control process as claimed in one of claims 2 to 11, characterized in that it consists, during the read phase (PHL), in applying to the photosensitive point a read pulse (IL) having the same sign as and an amplitude greater than or equal to the biasing pulse (IP).

13. The control process as claimed in one of claims 1 to 12, characterized in that the switching element is a diode (Dc).

14. The control process as claimed in one of claims 1 to 12, characterized in that the switching element is a transistor (T).

15. The control process as claimed in one of claims 1 to 14, the photosensitive point being produced on a first face of a substrate (7) transparent to light, characterized in that it consists in applying the optical flashes to the photosensitive point through the transparent substrate.

16. The control process as claimed in one of claims 2 to 15, characterized in that it consists in using the same source (SL) in order to deliver the optical flashes and the optical erasure flux.

17. A photosensitive device implementing the control process as claimed in any one of claims 1 to 16, comprising at least one photosensitive point (P1 to P9) with a photodiode (Dp) connected to a switching element (Dc), characterized in that it comprises means (SL) for exposing the photosensitive point to a series of periodic optical flashes (FO) and means (3, 13) to reverse bias the photodiode at the end of an optical flash so that it is in a receptive state from the start of the second imaging cycle.

18. The device as claimed in claim 17, characterized in that the means to reverse bias the photodiode make it possible to apply to the photosensitive point a biasing pulse during the exposure to the series of optical flashes.

19. The device as claimed in either of claims 17 and 18, characterized in that the switching element is a diode.

20. The device as claimed in either of claims 17 and 18, characterized in that the switching element is a transistor.

21. The device as claimed in one of claims 17 to 20, characterized in that the photosensitive point is produced on a first face of a substrate (7) transparent to light and in that it comprises a source (SL) for delivering the optical flashes (FO), placed on the second face of the substrate.

22. The photosensitive device as claimed in one of claims 17 to 21, characterized in that it comprises a scintillator (9) converting X-ray radiation incident on taking the image into optical radiation, the photodiode being sensitive to the optical radiation.

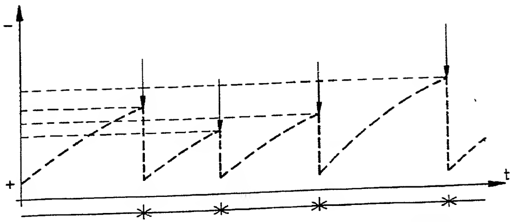


FIG.1a

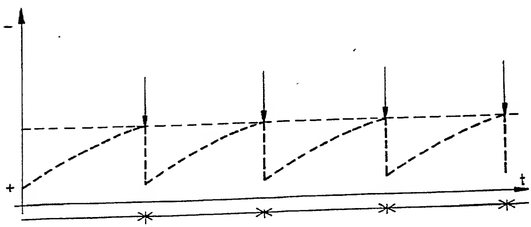


FIG.1b

FIG. 2

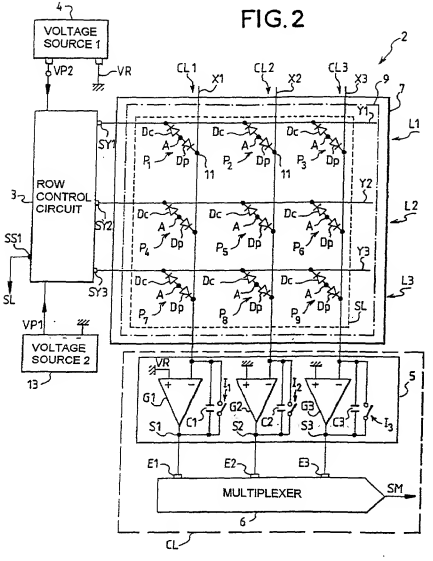
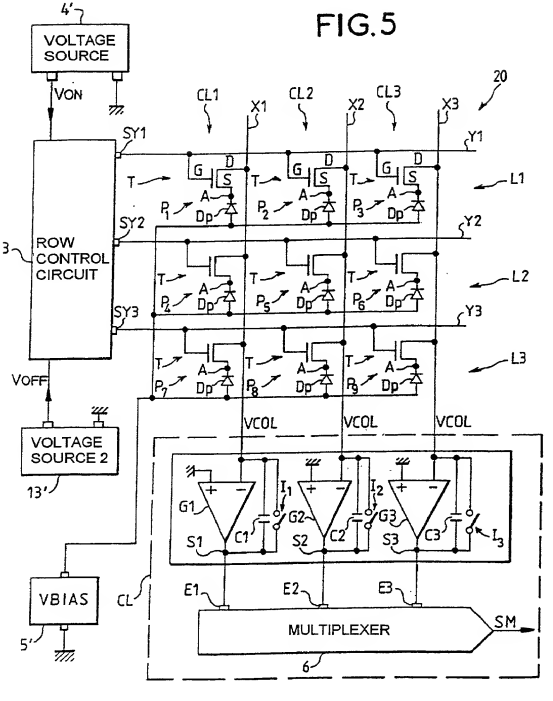

4
VOLTAGE SOURCE 1
VP2
VR
CL1
CL2
CL3
X1
X2
X3
2
9
7
Y1
Y2
Y3
L1
L2
L3
ROW CONTROL CIRCUIT
3
SY1
SY2
SY3
SS1
SL
VP1
VOLTAGE SOURCE 2
13
Dc
A
Dp
P1
P2
P3
P4
P5
P6
P7
P8
P9
11
5
G1
G2
G3
C1
C2
C3
I1
I2
I3
S1
S2
S3
E1
E2
E3
MULTIPLEXER
SM
6
CL

FIG.3a
FIG.3b
FIG.3c
FIG.3d
FIG.3e
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9,t10
t11
t'1
VR
VP1
VP2
IP
IL
FD
FE
dt dt dt dt
VAS
VA2
VA7
VA6
VA4
VA3
VAI
IMAGE REQUEST
OPEN
CLOSED
PHL
PHER
PHM
IMAGING CYCLE

FIG.4a
FIG.4b
FIG.4c
FIG.4d
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
VR
VP1
VP2
IL
IP
IPI
IFP
FE
FO
PHL
PHI
PHM
PHER
IMAGING CYCLE
VA

FIG.5


4'
VOLTAGE SOURCE
VON
SY1
SY2
SY3
3
ROW CONTROL CIRCUIT
VOFF
VOLTAGE SOURCE 2
13'
VBIAS
5'
CL
CL1
CL2
CL3
X1
X2
X3
20
Y1
Y2
Y3
L1
L2
L3
T
G
D
S
A
Dp
P1
P2
P3
P4
P5
P6
P7
P8
P9
VCOL
VCOL
VCOL
G1
G2
G3
C1
C2
C3
S1
S2
S3
I1
I2
I3
E1
E2
E3
MULTIPLEXER
SM
6

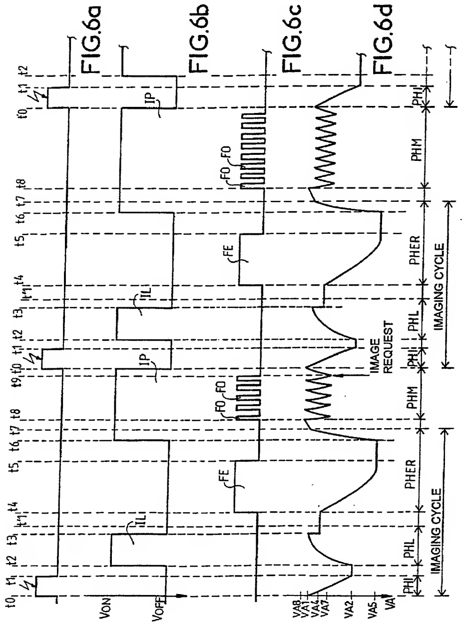


FIG.6a

FIG.6b

FIG.6c

FIG.6d

Declaration and Power of Attorney for Patent Application
Déclaration et Pouvoirs pour Demande de Brevet

French Language Declaration

En tant l'inventeur nommé ci-après, je déclare par le présent acte que:

As a below named inventor, I hereby declare that:

Mon domicile, mon adresse postale et ma nationalité sont ceux figurant ci-dessous à côté de mon nom.

My residence, post office address and citizenship are as stated next to my name.

Je crois être le premier inventeur original et unique (si un seul nom est mentionné ci-dessous), ou l'un des premiers co-inventeurs originaux (si plusieurs noms sont mentionnés ci-dessous) de l'objet revendiqué, pour lequel une demande de brevet a été déposée concernant l'invention intitulée

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PROCESS FOR CONTROLLING A PHOTO-SENSITIVE DEVICE CAPABLE OF PRODUCING HIGH-QUALITY IMAGES

et dont la description est fournie ci-joint à moins

the specification of which:

☐ ci-joint

☐ a été déposée le _____

sous le numéro de demande des Etats-Unis ou le numéro de demande international PCT

_____ et modifiée le

_____ (le cas échéant).

☐ is attached hereto.

☒ was filed on June 27, 2000

as United States Application Number or PCT International Application Number

PCT/FR00/01795 and was amended on

_____ (if applicable).

Je déclare par le présent acte avoir passé en revue et compris le contenu de la description ci-dessus, revendications comprises, telles que modifiées par toute modification dont il aura été fait référence ci-dessus.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

Je reconnais devoir divulguer toute information pertinente à la brevetabilité, comme défini dans le Titre 37, § 1.56 du Code fédéral des réglementations.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

French Language Declaration

Je revendique par le présent acte avoir la priorité étrangère, en vertu du Titre 35, § 119(a)-(d) ou § 365(b) du Code des Etats-Unis, sur toute demande étrangère de brevet ou certificat d'inventeur ou, en vertu du Titre 35, § 365(a) du même Code, sur toute demande internationale PCT désignant au moins un pays autre que les Etats-Unis et figurant ci-dessous et, en cochant la case, j'ai aussi indiqué ci-dessous toute demande étrangère de brevet, tout certificat d'inventeur ou toute demande internationale PCT ayant une date de dépôt précédant celle de la demande à propos de laquelle une priorité est revendiquée

I hereby claim foreign priority under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below, and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
Demande(s) de brevet antérieure(s) dans un autre pays.

			Priority claimed / Droit de priorité revendiqué	
99 08707	FRANCE	6 JULY 1999	☒ Yes / Oui	☐ No / Non
(Number) / (Numéro)	(Country) / (Pays)	(Day/Month/Year Filed) / (Jour/Mois/Anné de dépôt)		
			☐ Yes / Oui	☐ No / Non
(Number) / (Numéro)	(Country) / (Pays)	(Day/Month/Year Filed) / (Jour/Mois/Anné de dépôt)		

Je revendique par le présent acte tout bénéfice, en vertu du Titre 35, § 119(e) du Code des Etats-Unis, de toute demande de brevet provisoire effectuée aux Etats-Unis et figurant ci-dessous

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application No.) / (N° de demande)	(Filing Date) / (Date de dépôt)	(Application No.) / (N° de demande)	(Filing Date) / (Date de dépôt)

Je revendique par le présent acte tout bénéfice, en vertu du Titre 35, § 120 du Code des Etats-Unis, de toute demande de brevet effectuée aux Etats-Unis, ou en vertu du Titre 35, § 365(c) du même Code, de toute demande internationale PCT désignant les Etats-Unis et figurant ci-dessous et, dans la mesure où l'objet de chacune des revendications de cette demande de brevet n'est pas divulgué dans la demande antérieure américaine ou internationale PCT, en vertu des dispositions du premier paragraphe du Titre 35, § 112 du Code des Etats-Unis, je reconnais devoir divulguer toute information pertinente à la brevetabilité, comme défini dans le Titre 37, § 1.56 du Code fédéral des réglementations, dont j'ai pu disposer entre la date de dépôt de la demande antérieure et la date de dépôt de la demande nationale ou internationale PCT de la présente demande:

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application No.) / (N° de demande)	(Filing Date) / (Date de dépôt)	(Status) (patented, pending, abandoned) / (Statut) (breveté, en cours d'examen, abandonné)
PCT/FR00/01795	June 27, 2000	
(Application No.) / (N° de demande)	(Filing Date) / (Date de dépôt)	(Status) (patented, pending, abandoned) / (Statut) (breveté, en cours d'examen, abandonné)

Je déclare par le présent acte que toute déclaration ci-incluse est, à ma connaissance, véridique et que toute déclaration formulée à partir de renseignements ou de suppositions est tenue pour véridique, et de plus, que toutes ces déclarations ont été formulées en sachant que toute fausse déclaration volontaire ou son équivalent est passible d'une amende ou d' une incarcération, ou des deux, en vertu de la Section 1001 du Titre 18 du Code des Etats-Unis, et que de telles déclarations volontairement fausses risquent de compromettre la validité de la demande de brevet ou du brevet délivré à partir de celle-ci.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

French Language Declaration

POUVOIRS: En tant que l'inventeur cité, je désigne par la présente l'(les) avocat(s) et/ou agent(s) suivant(s) pour qu'ils poursuive(nt) la procédure de cette demande de brevet et traite(nt) toute affaire s'y rapportant avec l'Office des brevets et des marquees: *(mentionner le nom et le numéro d'enregistrement).*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

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(Supply similar information and signature for third and subsequent joint inventors.)

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Nom complet du sixième co-inventeur, le cas echeant	Full name of sixth joint inventor, if any Paul APARD
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